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Date: May 8, 2006

Brooke French

In re application of: **Emmot, et al**

Confirmation No.: **5465**

U.S. Serial Number: **10/644,215**

Art Unit: **2671**

Filing Date: **August 20, 2003**

Examiner: **Tung, Kee M.**

Our Reference Number: **10001763-1 (50817-1500)**

Title: **System and Method for Communicating Information from a Single-Threaded Application over Multiple I/O Busses**

Appeal Brief Transmittal
Appeal Brief

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PATENT APPLICATION

ATTORNEY DOCKET NO. 10001763-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Emmot, et al

Application No.: 10/644,215

Filing Date: August 20, 2003

Confirmation No.: 5465

Examiner: Tung, Kee M.

Group Art Unit: 2671

Title: System and Method for Communicating Information from a Single-Threaded Application over Multiple I/O Busses

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on March 9, 2006.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120 ☐ 2nd Month $450 ☐ 3rd Month $1020 ☐ 4th Month $1590

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 500. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Typed Name: Brooke French
Signature:

Respectfully submitted,

By

Daniel R. McClure
Attorney/Agent for Applicant(s)
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Rev 10/05 (AplBrief)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	)	
	)	
Emmot, et al	)	Group Art Unit: 2671
	)	
Serial No.: 10/644,215	)	Examiner: Tung, Kee M.
	)	
Filed: August 20, 2003	)	Confirmation No.: 5465
	)	
For: System and Method for Communicating Information from a Single-Threaded Application over Multiple I/O Busses	)	TKHR Docket: 50817-1500 HP Ref: 10001763-1

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APPEAL BRIEF UNDER 37 C.F.R. §1.192

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Sir:

This is an appeal from the decision of Examiner Kee M. Tung, Group Art Unit 2671, mailed January 12, 2006, rejecting claims 1-16 in the present application and making the rejection FINAL.

I. REAL PARTY IN INTEREST

The real party in interest of the instant application is Hewlett-Packard Development Company, a Texas Limited Liability Partnership having its principal place of business in Houston, Texas.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

Claim 1-16 are pending in this application, and all claims were rejected by the FINAL Office Action and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

All claim amendments submitted before the mailing date of the FINAL Office Action have been entered, and no claim amendments have been submitted subsequent to the mailing of the FINAL Office Action. In response to the FINAL Office Action, Applicant submitted a non-substantive amendment to the specification. A copy of the current claims is attached hereto as Appendix A.

On page 2 of the FINAL Office Action, the Examiner notes issues with claims 11 and 12. This was the first time that the Examiner raised the noted issues, and these claims have not been amended since the original filing of this application. Applicant will file a corrective amendment to the noted informalities, after receiving the decision on appeal.

Likewise, the Examiner has maintained an objection to the drawings. Title 35 U.S.C. § 113 "Drawings" states: "The applicant shall furnish a drawing where necessary for the understanding of the subject matter sought to be patented...." The Examiner relies on 37 C.F.R. § 1.83(a) (as apparently preempting the statutory provision of 35 U.S.C. § 113) to maintain that the drawings must separately illustrate each and every feature that is presented in the patent claims. In this regard, the Examiner objects to the drawings as failing to show the "partitioning logic" of claims 7 and 10-11 (even though the specification describes the function of the partitioning logic as being part of the "Chip Set" 218, which is illustrated in FIGs. 3 and 4). Applicant submits that adding a separate block, labeled as "partitioning logic," as a sub-block to the chip set 218 is not "necessary for the understanding of the subject matter sought to be patented" and as such is not required by the patent statutes. Notwithstanding, and to advance the prosecution of this application, Applicants will amend the drawings to add a separate block (labeled "partitioning logic") as being a part of the chip set 218, after receiving the decision on appeal.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Embodiments of the claimed subject matter are illustrated in FIGs. 2 through 5 and are discussed in the specification at least at pages 4-10.

Embodiments of the invention, such as those defined by claim 1, define a method comprising partitioning (see e.g., FIG. 5, reference numeral 402 and related description) state-sequenced information for communication to a computer subsystem (see e.g., FIG. 4, reference numeral 230 and related description); communicating the partitioned information (see e.g., FIG. 5, reference numeral 404 and related description) to the subsystem over a plurality of

input/output busses (see e.g., FIG. 4, reference numerals 242, 244, and 246 and related description); and separately processing (see e.g., FIG. 5, reference numeral 406 and related description) partitioned information received over each of the plurality of input/output busses, without first re-sequencing the information.

Embodiments of the invention, such as those defined by claim 2, further define the method of claim 1, wherein the separately processing processing (see e.g., FIG. 5, reference numeral 406 and related description) further comprises obtaining state information from the received information (*see e.g.*, p. 7, line 5 through p. 8, line 7), and processing the information in a proper state context.

Embodiments of the invention, such as those defined by claim 7, define computer system (see e.g., FIG. 4 and related description) comprising a host processor (see e.g., FIG. 4, reference numeral 210 and related description) configured to execute a single-threaded application (see e.g., FIG. 4, reference numeral 212 and related description); partitioning logic for partitioning state-sequenced information (see e.g., FIG. 4, reference numeral 218 and related description – including p. 9, paragraph 0029); communication logic (see e.g., paragraphs 0020-0025) configured to communicate partitioned state-sequenced information across a plurality of input/output busses (see e.g., FIG. 4, reference numerals 242, 244, 246 and related description); a plurality of interfaces (see e.g., FIG. 4, reference numerals 232, 234, and 236 and related description) located at a subsystem (see e.g., FIG. 4, reference numeral 230 and related description) for receiving the information communicated across the plurality of the input/output busses; processing logic (see e.g., FIG. 4, reference numeral 238 and related description) for controlling the processing of the partitioned information without re-sequencing the information, the processing logic configured to preserve state information of the information processed.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The FINAL Office Action rejected claims 1-15 under 35 U.S.C. § 103(a) as allegedly obvious over the combination of U.S. Patent No. 6,801, 202 to Nelson (hereafter Nelson) in view of U.S. Patent No. 6,311,247 to Spencer (hereafter Spencer).

The FINAL Office Action also rejected claim 16 under 35 U.S.C. § 103(a) as allegedly unpatentable over Nelson and Spencer in further view of U.S. Patent No. 6,924,807 to Ebihara (hereafter Ebihara).

VII. ARGUMENT

New Rejection

The FINAL Office Action (p. 3), for the first time during the pendency of this application, rejected claim 10 under 35 U.S.C. § 112, first paragraph as allegedly failing to comply with the written description requirement. The undersigned believes this rejection results from an informality with claim 10, in which the term "at" should be deleted. After receiving the decision on appeal, the undersigned will amend claim 10 to correct this informality. Notwithstanding, as claim 10 has never been amended during the prosecution of this application, the undersigned does not understand why this new ground of rejection is being first raised in an Office Action made FINAL. Either the new rejection or the status of FINAL is improper.

Discussion of Art-based Rejections - (Independent claims 1 and 7 and dependent claims 2-6 and 8-16)

Turning now to the art-based rejections, the FINAL Office Action has continued to reject all claims 1-16 on identical bases as were set forth in the previous, non-final Office Action. Specifically, the FINAL Office Action has rejected claims 1-15 as allegedly unpatentable over the combination of Nelson in view of Spencer. Further, the Office Action has rejected claim 16 under 35 U.S.C. § 103(a) as allegedly unpatentable over Nelson and Spencer in further view of Ebihara. For at least the reasons set forth herein, Applicants respectfully disagree with the rejections and request that the rejections be overturned.

The FINAL Office Action alleged that:

> Spencer teaches a computer system (Fig. 2) comprising a host processor (112) configured to execute a single-threaded application; partitioning logic (123) for partitioning the state-sequenced information, communication logic (chipset 120) configured to communication partitioned state-sequenced information across a plurality of I/O busses (PCI buses 116-118); a plurality of interfaces (124-128) located at a subsystem for receiving the information communication across the plurality of I/O busses; processing logic (not shown, but would have been obvious to connect any peripheral (I/O) devices into the PCI busses 116-118, for example, graphics processor is considered one of the peripheral device) for controlling the processing of the partitioned information without re-sequencing the information, the processing logic configured to preserve state information of the information processed.

This is, in fact, not what Spencer teaches. Instead, Spencer is directed to a system and method for interfacing a system bus to a plurality of PCI busses. As is described in Spencer, previous systems interfaced with external PCI devices via a shared PCI bus. The system of Spencer provides multiple PCI busses, which are dedicated to different devices and allow communications to each device to take place over a dedicated PCI bus. Figure 4 of the Spencer reference illustrates an embodiment of an architecture for interfacing a system bus with such multiple PCI busses or PCI bus interfaces.

Returning to the application of Spencer (quoted above) made by the Office Action, the Office Action stated that "Spencer teaches...a host processor (112) configured to execute a single-threaded application; partitioning logic (123) for partitioning the state-sequenced information..." First, there is no teaching in Spencer of the host processor being "configured to execute a singe-threaded application." As noted above, and as is specifically taught in Spencer, the embodiments described therein relate to the interfacing of a system bus interface with multiple PCI bus interfaces. The application being executed on the host processor could be a single-threaded application, or could be a multi-threaded application (Spencer is simply silent on this point, as it is not a feature germane to that disclosure). The FINAL Office Action responded to this point by alleging that "it would have been obvious to one of ordinary skill in the art to implement Spencer because both single-threaded or multi-threaded provide advantages..." In making this allegation, the Office Action appears to reflect a misunderstanding (or lack of appreciation) for the claimed invention. In this regard, a significant feature of the claimed embodiments it the communication of partitioned information from a SINGLE-threaded application over MULTIPLE I/O busses to a subsystem (where the partitioned information is executed without first being reassembled). The Office Action avoids specifically addressing this significant feature by simply alleging (generally) that it would have been obvious (as though single-threaded and multi-threaded application are interchangeable – which they are not , especially in the context of problems sought to be remedied by embodiments of the present invention). For at least this reason, the rejection is misplaced and should be overturned.

In addition, the Office Action alleged that Spencer discloses "partitioning logic (123) for partitioning state-sequenced information..." Reference numeral 123 of Spencer is illustrated in Figure 4 and broadly denotes an architecture of an embodiment of an I/O controller (see column

5, line 15). The function of this architecture is to interface the system bus interface with multiple PCI bus interfaces for both incoming and outgoing PCI communications. Significantly, there is absolutely no teaching or suggestion in Spencer relating to the partitioning of state-sequenced information, as this is not a feature that is germane to the disclosure of Spencer. For at least this reason, the Office Action's application of Spencer to the embodiments of the invention that are defined in each of the independent claims is misplaced.

In this regard, independent claims 1 and 7 recite:

> 1. A method comprising:
> ***partitioning state-sequenced information for communication to a computer subsystem;***
> communicating the partitioned information to the subsystem over a plurality of input/output busses; and
> ***separately processing partitioned information received over each of the plurality of input/output busses, without first re-sequencing the information.***
>
> 7. A computer system comprising:
> a host processor configured to execute a single-threaded application;
> ***partitioning logic for partitioning state-sequenced information,***
> communication logic configured to communicate partitioned state-sequenced information across a plurality of input/output busses;
> a plurality of interfaces located at a subsystem for receiving the information communicated across the plurality of the input/output busses;
> ***processing logic for controlling the processing of the partitioned information without re-sequencing the information, the processing logic configured to preserve state information of the information processed.***

(*Emphasis added.*) As emphasized above, independent claim 1 includes, among other features, "partitioning state-sequenced information for communication to a computer subsystem." Likewise, claim 7 defines "partitioning logic for partitioning state-sequenced information." There is simply no disclosure or suggestion in Spencer (as alleged by the FINAL Office Action) of these claimed features. For at least this reason, the rejections of independent claims 1 and 7

are misplaced and should be overturned. For at least the same reasons, all remaining claims 2-6 and 8-16, which depend from independent claims 1 and 7, respectively, should be overturned as well.

Further, with regard to independent claim 7, this claim recites "processing logic for controlling the processing of the partitioned information without re-sequencing the information, the processing logic configured to preserve state information of the information processed." On page 5, lines 2-4 of the FINAL Office Action, the FINAL Office Action admits that this processing logic is not shown in Spencer, but instead alleges that it would have been obvious. Applicants respectfully disagree. In fact, the reason that such logic is neither illustrated nor suggested in Spencer is that such logic would be completely counter to the objective of the invention of Spencer. As noted above, Spencer is directed to a system and method for interfacing a system bus interface with multiple PCI bus interfaces. In doing so, a host computer can communicate directly, over dedicated PCI busses, to multiple devices that communicate via a PCI bus. Even assuming, for the sake of argument, that Spencer showed the partitioning of state-sequenced information and the communication of that information over the independent PCI busses to multiple PCI devices, each such device would thereafter perform its operations independently of the other PCI devices and therefore would have no reason or need to re-sequence any state-sequenced information. Indeed, the fact that the PCI devices are devices that operate independently underscores the fact that the information being sent to these devices independently does not originate from state-sequenced information.

For example, and as disclosed in Spencer, examples of PCI devices include "disc drive controllers, video cards, modems or other communication devices, etc." (Spencer, column 6, lines 27-28). The undersigned respectfully submits that a person skilled in the art would

recognize that information sent to a disc drive controller, would not be linked, in a state-sequenced fashion, with information sent to devices like video cards, modems, etc. Accordingly, a person skilled in the art would not construe the teachings of Spencer to include, implicitly or inherently, either logic to partition state-sequenced information for communication over PCI busses or logic configured to process the partitioned information while preserving state information of the information processed (as alleged by the Office Action). For at least this additional reason, the rejection of independent claim 7 (as well as dependent claims 8-16) is misplaced and should be overturned.

Similarly, the feature of dependent claim 2 calls for "obtaining state information from the received information, and processing the information in a proper state context." The Office Action has not even alleged, with specificity, that this claimed feature is taught in any of the cited art. In this regard, in rejecting claim 2, the Office Action merely stated that "claims 1, 2, and 4-6 are similar in scope to system claims 7-15 above and thus are rejected under similar rationale." (Office Action, page 5, lines 9-10). However, the feature just quoted from claim 2 is not referenced anywhere in the Office Action's rejection of claim 7.

Applicant made this argument in response to the non-final Office Action. The FINAL Office Action responded (p. 8, last paragraph) simply by alleging that this feature "would have been obvious in view of the teachings of processing logic of Spencer and Nelson because both the processing logic receiving information from host computer and processing the data based on the information (data and command) received from the host computer." Again, rather than specifically point to teachings of the claimed feature, the Office Action merely alleged that it would have been obvious. This type of general, unsupported rejection, if permitted to stand, could be used to reject virtually any claim ever presented for examination. Title 35 U.S.C. §

103(a) requires more than this. Accordingly, and for at least this additional reason, the rejection of claim 2 is misplaced and should be overturned.

As a separate and independent basis for the patentability of all claims, the undersigned further submits that the Office Action's application of the Nelson reference is similarly misplaced. In this regard, the system of Nelson is directed to a graphics system that is configured to perform parallel processing of graphics data using multiple graphics pipelines. Significantly, rather than partitioning [graphics] information for communication over multiple I/O busses, as required by the claims of the present invention, Nelson merely describes the division of graphics information into a plurality of "rendering units" (reference numbers 150A-150D). In fact, Fig. 3 of Nelson illustrates a control unit 140 that interfaces to a computer system via a single high-speed bus (not multiple I/O busses). Once the information is received by the control unit 140, it is split among a plurality of rendering units for processing. This parallel processing is simply inapplicable to the features of the claimed embodiments of the invention, which call for the partitioning of state-sequenced information for communication over a plurality of I/O busses, and the subsequent processing of the state-sequencing information without first re-sequencing the data. As noted above, the alleged teachings of Spencer for allegedly disclosing the multiple I/O busses and the processing of state-sequenced information is misplaced. For at least this separate and independent reason, the rejection of independent claims 1 and 7 are misplaced and should be overturned.

Separate and independent basis for patentability of all claims

As a separate and independent basis for the patentability of these claims, Applicants

respectfully submit that the Office Action has failed to cite a proper suggestion or motivation for combining Spencer with Nelson. In combining these references, the Office Action stated only that the combination would have been obvious "because multiple separate busses allows exclusive communication by providing a direct pipe therebetween and thus provides significant performance enhancements over prior art systems that have shared PCI busses as taught by Spencer (abstract)." First, this cited teaching from Spencer refers to the advantage of providing dedicated PDI busses between a device and multiple devices that intercommunicate with the device over PCI busses. However, it does NOT suggest the modification of the parallel processing pipelined architecture of Nelson to have multiple I/O busses.

Further, the alleged motivation is clearly improper in view of well-established Federal Circuit precedent. It is well-settled law that in order to properly support an obviousness rejection under 35 U.S.C. § 103, there must have been some teaching in the prior art to suggest to one skilled in the art that the claimed invention would have been obvious. W. L. Gore & Associates, Inc. v. Garlock Thomas, Inc., 721 F.2d 1540, 1551 (Fed. Cir. 1983). More significantly,

> "The consistent criteria for determination of obviousness is whether the prior art would have suggested to one of ordinary skill in the art that this [invention] should be carried out and would have a reasonable likelihood of success, viewed in light of the prior art. ..." Both the suggestion and the expectation of success must be founded in the prior art, not in the applicant's disclosure... In determining whether such a suggestion can fairly be gleaned from the prior art, the full field of the invention must be considered; for the person of ordinary skill in the art is charged with knowledge of the entire body of technological literature, including that which might lead away from the claimed invention."

(*Emphasis added.*) In re Dow Chemical Company, 837 F.2d 469, 473 (Fed. Cir. 1988).

In this regard, Applicants note that there must not only be a suggestion to combine the functional or operational aspects of the combined references, but that the Federal Circuit also requires the prior art to suggest both the combination of elements and the structure resulting from

the combination. Stiftung v. Renishaw PLC, 945 Fed.2d 1173 (Fed. Cir. 1991). Therefore, in order to sustain an obviousness rejection based upon a combination of any two or more prior art references, the prior art must properly suggest the desirability of combining the particular elements to derive a system and method for communicating state-sequenced information over multiple I/O busses, as claimed by the Applicants.

When an obviousness determination is based on multiple prior art references, there must be a showing of some "teaching, suggestion, or reason" to combine the references. Gambro Lundia AB v. Baxter Healthcare Corp., 110 F.3d 1573, 1579, 42 USPQ2d 1378, 1383 (Fed. Cir. 1997) (also noting that the "absence of such a suggestion to combine is dispositive in an obviousness determination").

Evidence of a suggestion, teaching, or motivation to combine prior art references may flow, inter alia, from the references themselves, the knowledge of one of ordinary skill in the art, or from the nature of the problem to be solved. See In re Dembiczak, 175 F.3d 994, 1000, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form, must nevertheless be "clear and particular." Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617.

If there was no motivation or suggestion to combine selective teachings from multiple prior art references, one of ordinary skill in the art would not have viewed the present invention as obvious. See In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); Gambro Lundia AB, 110 F.3d at 1579, 42 USPQ2d at 1383 ("The absence of such a suggestion to combine is dispositive in an obviousness determination.").

Significantly, where there is no apparent disadvantage present in a particular prior art

reference, then generally there can be no motivation to combine the teaching of another reference with the particular prior art reference. Winner Int'l Royalty Corp. v. Wang, No 98-1553 (Fed. Cir. January 27, 2000).

For at least the additional reason that the Office Action failed to identify proper motivations or suggestions for combining the various references to properly support the rejections under 35 U.S.C. § 103, the rejections of claims 1-15 should be overturned.

Similarly, the rejection of claim 16 should be overturned, as it has been rejected on even the more tenuous combination of Nelson and Spencer in further view of Ebihara. The Office Action alleged that this further combination would have been obvious "in order to provide synchronization among multiple graphics processors and thus to provide synchronized output signals." (Office Action, p. 6, lines 6-8). Applicants submit that this rationale is inconsistent with the relevant legal precedent set out above, and request that the rejection of claim 16 be overturned. Even more fundamentally, Ebihara fails to solve the deficiencies of the teachings of Nelson and Spencer, which have been set forth above.

The foregoing argument was advanced in response to the non-final Office Action. The FINAL Office Action responded by stating: "It is noted that basically, applicant argues the non-obviousness by attacking references individually where, as here the rejections are based on combination of references." (FINAL Office Action, p. 9) This mischaracterizes Applicants' arguments. In fact, Applicants argue the non-obviousness on separate and independent bases. First, Applicants note deficiencies in the application of the individual references (insofar as the references do not teach what the Examiner alleged that they teach). This misapplication of the references forms an independent basis for the patentability of all claims.

In addition, and independent of that argument, Applicants noted that the combination of

Nelson, Spencer, and Ebihara failed to satisfy the legal requirements for combining selective teachings from individual references.

CONCLUSION

Based upon the foregoing discussion, Applicant respectfully requests that the Examiner's final rejection of claims 1-16 be overturned by the Board, and that the application be allowed to issue as a patent with all pending claims 1-16.

In addition to the claims of Appendix A, Appendix B attached hereto indicates that there is no evidence being attached and relied upon by this brief. Appendix C attached hereto indicates that there are no related proceedings.

Please charge Hewlett-Packard Company's deposit account 08-2025 in the amount of $500 for the filing of this Appeal Brief. No additional fees are believed to be due in connection with this Appeal Brief. If, however, any additional fees are deemed to be payable, you are hereby authorized to charge any such fees to deposit account No. 08-2025.

Respectfully submitted,

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VIII. CLAIMS - APPENDIX

1. A method comprising:

partitioning state-sequenced information for communication to a computer subsystem;

communicating the partitioned information to the subsystem over a plurality of input/output busses; and

separately processing partitioned information received over each of the plurality of input/output busses, without first re-sequencing the information.

2. The method of claim 1, wherein the separately processing further comprises obtaining state information from the received information, and processing the information in a proper state context.

3. The method of claim 1, wherein the communicating partitioned state-sequenced information comprises performing at least one direct memory access (DMA) across each of the plurality of input/output busses.

4. The method of claim 1, wherein the communicating partitioned state-sequenced information comprises communicating the information over a peripheral component interface (PCI) bus.

5. The method of claim 1, wherein the information includes graphics information and the separately processing comprises performing graphics processing on the partitioned information.

6. The method of claim 1, wherein separately processing comprises performing an independent rendering on information received on each of the plurality of busses.

7. A computer system comprising:

a host processor configured to execute a single-threaded application;

partitioning logic for partitioning state-sequenced information,

communication logic configured to communicate partitioned state-sequenced information across a plurality of input/output busses;

a plurality of interfaces located at a subsystem for receiving the information communicated across the plurality of the input/output busses;

processing logic for controlling the processing of the partitioned information without re-sequencing the information, the processing logic configured to preserve state information of the information processed.

8. The system of claim 7, further comprising a buffer memory in communication with the host processor for storing state-sequenced information for communication to a subsystem.

9. The system of claim 7, wherein the processing logic is located at the subsystem.

10. The system of claim 7, wherein the partitioning logic is located in at the subsystem.

11. The system of claim 7, wherein the partitioning logic is located in at the at the host processor.

12. The system of claim 15, wherein the system is a computer graphics system.

13. The system of claim 7, wherein the processing logic comprises at least one geometry accelerator.

14. The system of claim 7, wherein each of the input/output busses are peripheral component interface (PCI) busses.

15. The system of claim 7, wherein the system comprises a plurality of processing nodes that are coupled through a communication network.

16. The system of claim 15, wherein the processing logic comprises work queues maintained among the processing nodes.

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IX. EVIDENCE - APPENDIX

None.

IX. RELATED PROCEEDINGS- APPENDIX

None.